

Figure 1

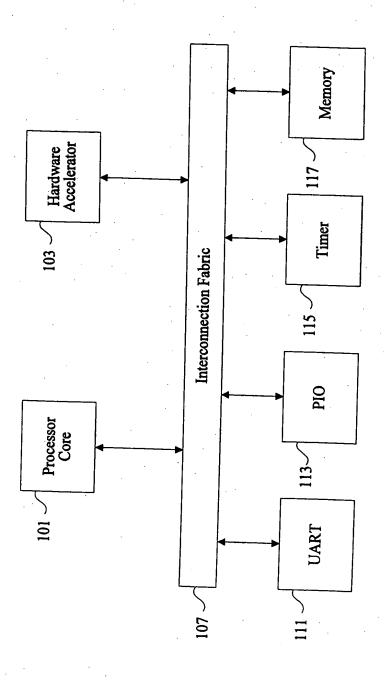


Figure 2

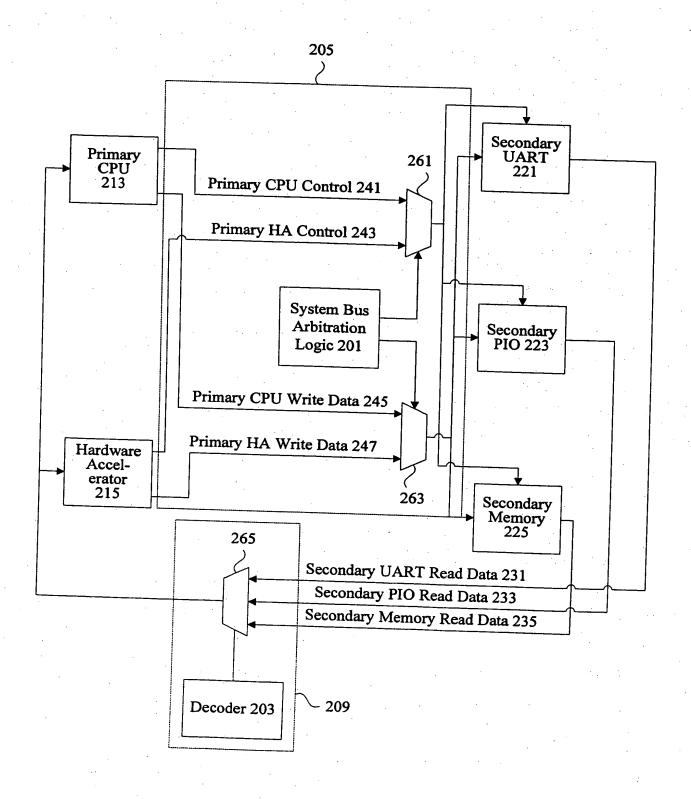


Figure 3

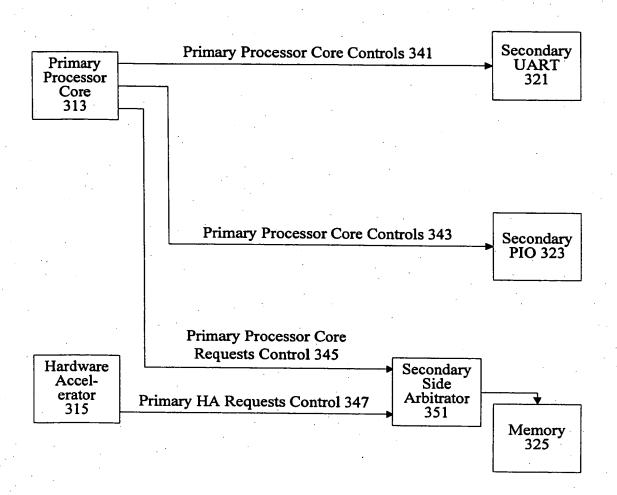


Figure 4

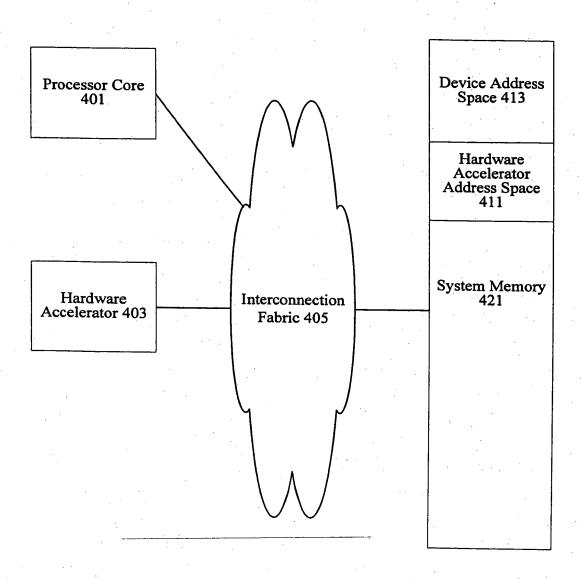


Figure 5

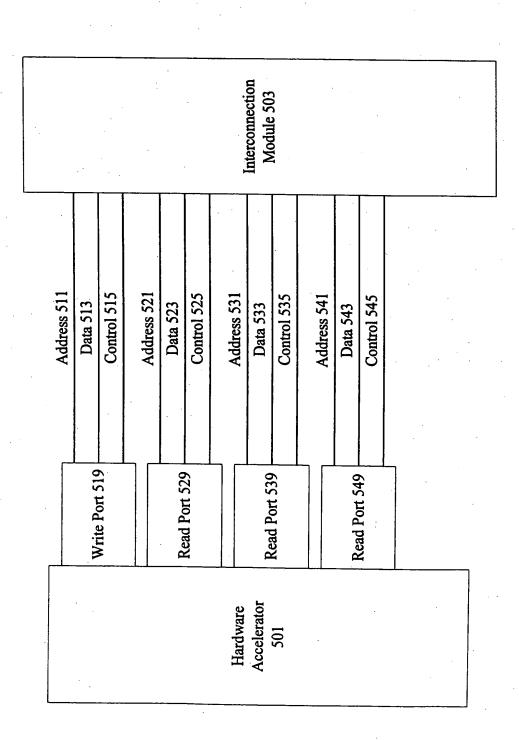


Figure 6

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	Secondary Component 605									
Clock 621	Address 623	Read 625	Chipselect 627	Wait Request 629	Data Valid 633					
	Interconnection Module 603									
	Address 611	Data 613	Control 616	Wait Request 617	Data Valid 619					
				Hardware	Accelerator 601					

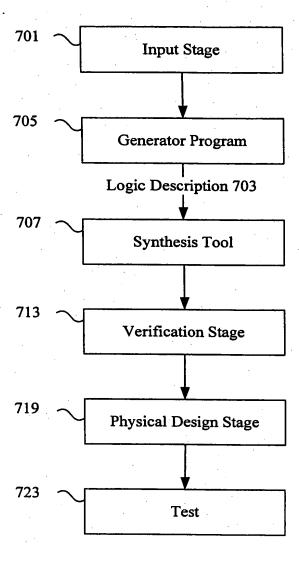


Figure 7

Figure 8

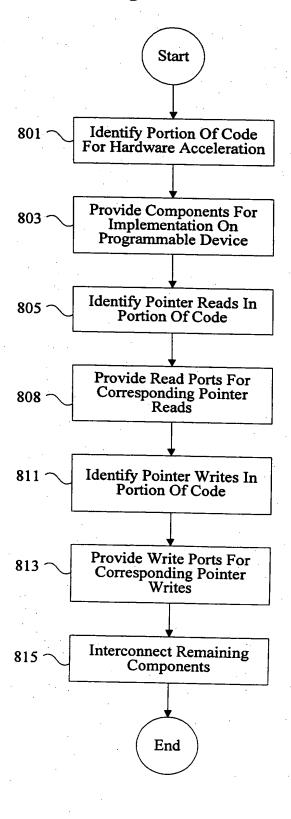
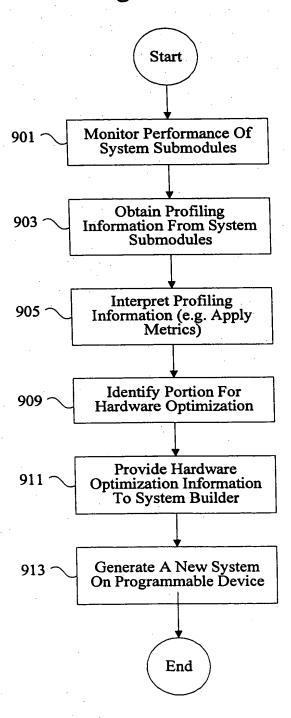


Figure 9



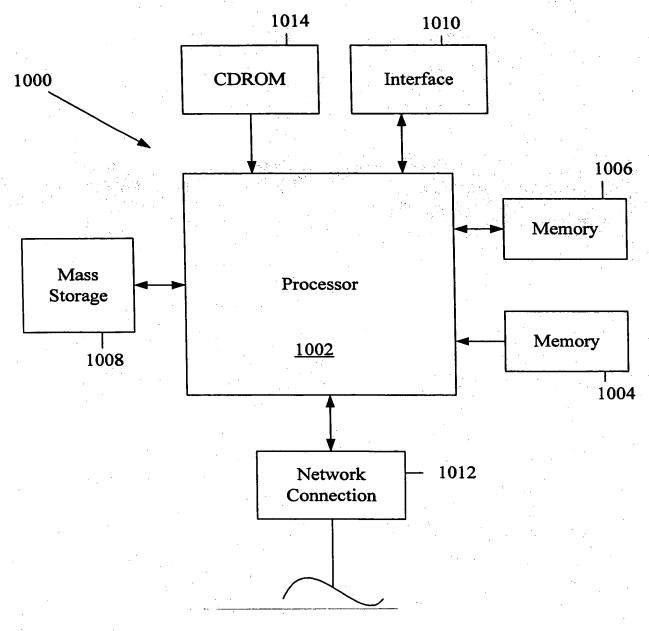


Figure 10